



## Low power flexible organic thin film transistors with amorphous Ba<sub>0.7</sub>Sr<sub>0.3</sub>TiO<sub>3</sub> gate dielectric grown by pulsed laser deposition at low temperature

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### ARTICLE INFO

#### Article history:

Received 29 December 2011

Received in revised form 18 March 2012

Accepted 19 March 2012

Available online 7 April 2012

#### Keywords:

Flexible organic transistor

High-k dielectric

Low operating power

Pulsed laser deposition

Bending test

### ABSTRACT

We deposited amorphous Ba<sub>0.7</sub>Sr<sub>0.3</sub>TiO<sub>3</sub> (BST) on silicon and plastic substrate under 110 °C by pulsed laser deposition (PLD) and use it as the dielectric of the organic transistor. Depends on the thickness of BST layer, the highest mobility of the devices can achieve 1.24 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> and 1.01 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> on the silicon and polyethylene naphthalate (PEN) substrate, respectively. We also studied the upward and downward bending tests on the transistors and the dielectric thin films. We found that the BST dielectric pentacene transistor can maintain the mobility at 0.5 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> or higher while the bending radius is around 3 mm in both upward and downward bending. Our finding demonstrates the potential application of PLD growth high-k dielectric in the large area organic electronics devices.

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Due to the flexibility, light weight and compatible with large area fabrication, organic electronics have received considerable attention in the past decades. Among different organic devices, organic thin film transistor (OTFT) have been considered as the key component in the plastic electronic circuits [1,2], and their applications cover active matrix display, radio frequency identification (RFID), memories or circuit processors [3–5]. In terms of device performance, although some OTFTs have shown comparable mobilities with amorphous silicon devices, it still need further reduction on the operating power of the devices especially for the battery-powered and portable devices, and a commonly adopted approach is by increasing the capacitance per unit area ( $C$ ) of the dielectric insulators. As the

$C$  is given by  $C = \epsilon\epsilon_0/t$  where  $\epsilon_0$  is the permittivity of vacuum,  $\epsilon$  and  $t$  are the dielectric constant and thickness of the insulator material, respectively; the value of  $C$  can be increased by either decreasing the thickness of the insulator layer or by employing an insulator with higher dielectric constant (high-k). The reduction of the thickness is challenging for low dielectric constant materials ( $\epsilon \leq 4$ ) such as PMMA or SiO<sub>2</sub> because it usually requires the dielectric layer to be extremely thin and the leakage current can be significant even if a small amount of defects exists. Self-assembly monolayers (SAMs) is an effective solution for reducing the dielectric thickness [6]. In the SAMs, the head group are specially designed for attaching onto particular gate dielectric insulator or gate electrodes by chemical bonding, while the terminating groups on the other hand control the growth morphology and the packing of the organic semiconductors (OSC). As the packing of the OSC affects the leakage current of the OTFTs, the terminating group hence also affects the leakage current. For example,

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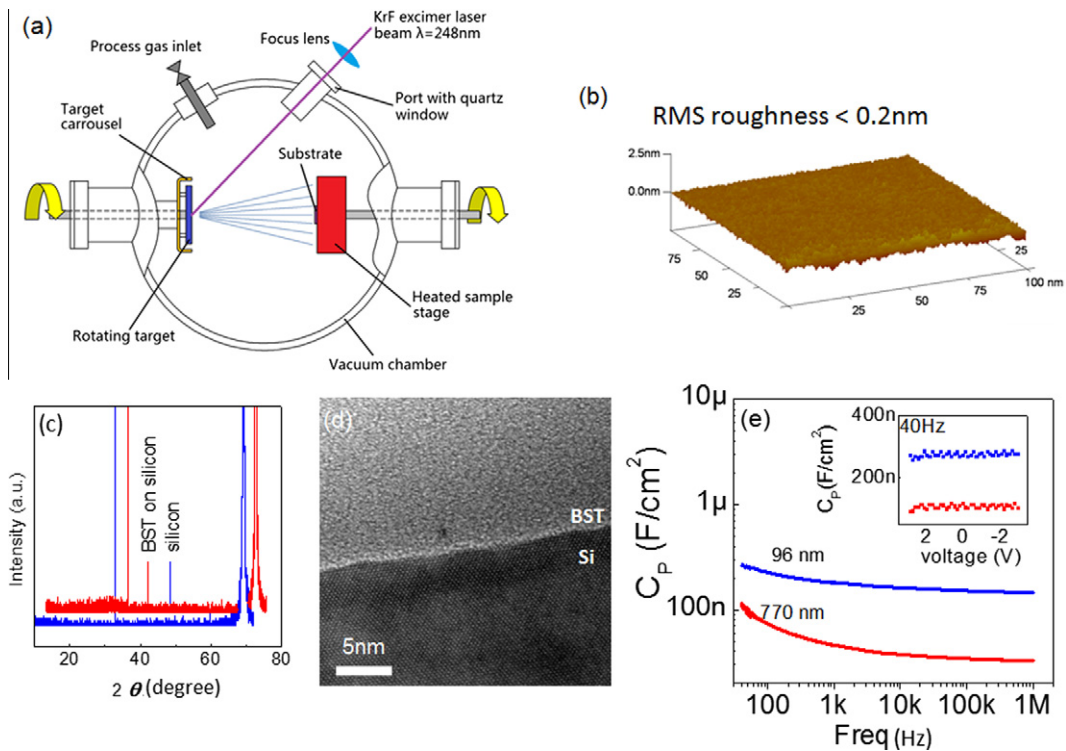
the leakage current of pentacene transistor with acene group as the terminating group shows 100 times reduction while comparing with the aromatic group [7]. However, as the head and terminating groups of the SAMs may only work for particular gate electrodes, dielectric insulators or organic semiconductors, different SAMs are required for various transistors; furthermore, it is also difficult to apply SAMs in the OTFTs with the top gate electrode configurations. On the other hand, for the employment of high permittivity dielectric insulators, OTFT fabricated on high- $k$  dielectric such as metal oxides have also shown their potentials on reducing the operating voltage. Pentacene OTFTs with aluminum oxide ( $\text{Al}_2\text{O}_3$ ) grown by sol-gel method [8], and hafnium oxide ( $\text{HfO}_2$ ) grown by atomic layer deposition [9] have shown low operating voltages at around 3 V, but the high processing and annealing temperature for solvent removal and crystallization of the dielectric may limit their applications on flexible substrates with low glass transition temperatures.

Similar to the sol-gel method with high annealing temperature ( $>700^\circ\text{C}$ ) [10], high substrate temperature pulsed laser deposition (PLD) is usually applied for growing crystalline  $\text{Ba}_{0.7}\text{Sr}_{0.3}\text{TiO}_3$  (BST) with high dielectric constant ( $\epsilon > 200$ ) and under low oxygen pressure environment [11]. Due to the ferroelectric properties of the crystalline BST films, they can be used as tunable capacitors [12], optical modulator [13] or microwave circuit components [14]. However, as the crystal grains and the boundaries hinder the growth of the organic semiconductors, it is difficult to apply crystalline BST as the OTFT dielectric insulators. To overcome the morphology effect induced by the crystalline BST, amorphous BST prepared by solution processing under lower annealing temperature ( $400^\circ\text{C}$ ) have been employed as dielectric of OTFT on silicon substrate [15]. Although the roughness of the dielectric surface is significantly reduced in the amorphous BST and the field effect mobility ( $\mu_{FE}$ ) of the pentacene can achieve  $0.16\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$  [15], the processing temperature is still too high for the plastic flexible substrates which usually have the glass transition temperatures at  $200^\circ\text{C}$  or lower. To overcome this, Dimitrakopoulos et al., also demonstrates the fabrication of amorphous barium zirconate titanate (BZT) by using room temperature magnetron sputtering method on flexible polycarbonate substrate [16]. The device shows a higher mobility ( $\mu_{FE} = 0.38\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ ) but the saturation properties in the output curves is weaker than the solution processing device and it could be due to the fact that larger surface roughness in the magnetron sputtering films hence larger leakage current in the device.

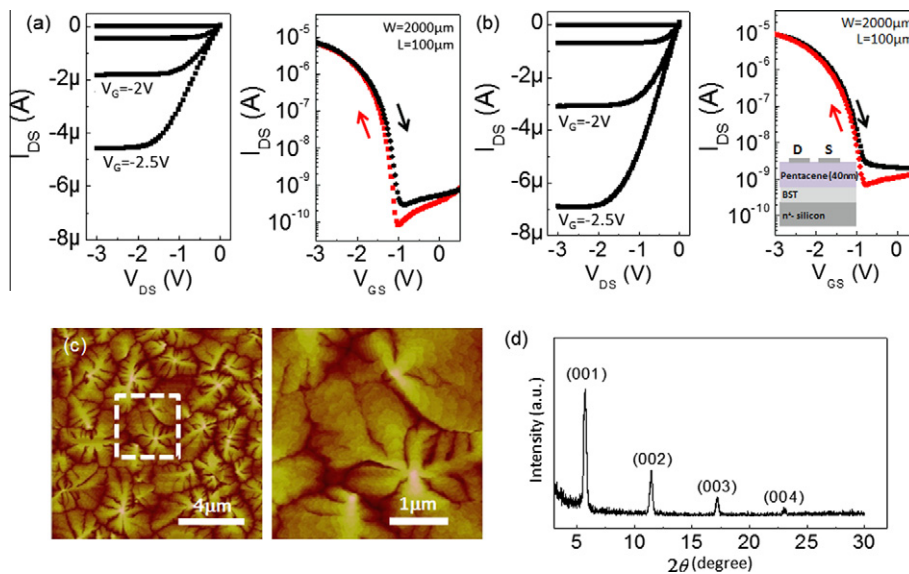
In this study, we demonstrated a low temperature high- $k$  dielectric processing technique which can be applied on plastic substrates. Low operating power OTFTs are fabricated on amorphous BST with a smooth surface (roughness  $<0.2\text{ nm}$ ). The BST thin films are grown by PLD under low processing temperature ( $110^\circ\text{C}$ ) and the capacitance per unit area of the thin films at low frequency can achieve ca.  $300\text{ nF cm}^{-2}$ . The pentacene OTFTs have threshold voltage around 1 V, field effect mobility as high as  $1.24\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$  (on silicon) and  $1.01\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$  (on flexible substrate), operating voltage  $<3\text{ V}$  and on/off ratio

$>1 \times 10^4$  (both silicon and flexible substrates). Although the current BST are deposited on silicon and polyethylene naphthalate (PEN) substrates with an area just  $6.55\text{ cm}^2$  ( $1\text{ in.} \times 1\text{ in.}$ ), the PLD deposition method has been demonstrated for deposition of thin films with a much larger area before [17,18]. Moreover, the BST dielectric is compatible with both top and bottom gate contact configurations, as well as various fabrication techniques other than thermal evaporation such as solution processing and vapor jet deposition [19]. To the best of our knowledge, it is the first demonstration of amorphous BST thin film grown by PLD at low temperature for flexible OTFT applications. The stable performance of the OTFT under bending test shows its potential for flexible electronics.

The PLD deposition of the BST is performed under pressure of  $2 \times 10^{-3}\text{ Pa}$  while the substrate holder keeps at  $110^\circ\text{C}$  as shown in the schematic diagram of the PLD system in Fig. 1(a). Low pressure environment is used for preventing the oxidization of the hydrofluoric acid treated silicon substrates. The 248 nm KrF excimer laser with a repetition frequency of 10 Hz, pulse width of 10–50 ns and the corresponding energy per pulse 250 mJ is used as the source. The distance between the target and the substrate holder is maintained at 5 cm and the thickness of the BST thin film is controlled by the growth time. Fig. 1(b) shows the atomic force microscope (AFM) (Digital Instrument, NanoScope VIII) image of the BST thin film deposited on heavily doped n-type silicon. It can be noticed that the amorphous BST film forms a smooth surface (RMS roughness is less than 0.2 nm). The amorphous nature is confirmed by the XRD (Rigaku Smartlab 9KW) measurements of the BST thin film on silicon substrate (Fig. 1(c)), where only peaks from the Si can be detected on the BST/Si substrate; it agrees with the results observed by Dong and co-workers [20]. To further investigate the interface quality between the silicon substrate and the BST thin film, we applied high resolution transmission electronic microscope (TEM) (Philips Tecnai G220 S-TWIN) to study the cross sectional image of the interface between the BST and Si substrate. As shown in Fig. 1(d), the amorphous BST is grown on the silicon evenly without crystallization and the amorphous nature of the BST can be clearly deviated from the highly crystallized silicon substrate. The dielectric properties of the BST thin films are characterized by  $C$ - $f$  measurements under the metal-insulator-metal (MIM) structure, in which  $600\text{ }\mu\text{m}$  diameter circular Ag top contacts are thermal evaporated onto the BST thin film on the n<sup>+</sup>-Si substrate. As shown in Fig. 1(e), the areal capacitances of the thinnest (96 nm) and thickest (770 nm) BST films used in our experiment maintain at relative constant values in the high frequency regime from 10 kHz to 1 MHz. However, in the low frequency regime, the capacitance of the 96 nm film increases from  $180\text{ nF cm}^{-2}$  at 1000 Hz to  $261\text{ nF cm}^{-2}$  at 40 Hz. The increase of capacitance at lower frequency regime of the 770 nm BST film is more significant and the capacitance increases from  $46\text{ nF cm}^{-2}$  at 1000 Hz to  $114\text{ nF cm}^{-2}$  at 40 Hz. It is interesting to notice that the capacitance decrease of the films is not proportional to the film thickness which suggests varying combination in thicker films and dead layer effect may exist in the films [21]. The increase



**Fig. 1.** (a) The schematic diagram of the pulsed laser deposition system. (b) AFM image of the BST thin film under tapping mode. (c) XRD results of the silicon substrate and the BST film on silicon. (d) High resolution TEM cross sectional image of the BST thin on silicon substrate, the amorphous nature of the BST can be clearly deviated from the crystalline silicon. (e) The  $C$ - $f$  characteristic curves of the BST thin films with thickness 96 nm and 770 nm. The inset is the  $C$ - $V$  characteristic curves of the same films.



**Fig. 2.** (a) The output and transfer curves of the OTFT with (a) 96 nm BST and (b) 770 nm BST on silicon. Inset of (b) shows the schematic diagram of the device structure. The active region pentacene layer is 40 nm thick and the drain (D), source (S) electrodes are 50 nm Ag. (c) (left) The AFM images of the pentacene thin film on the 770 nm BST. (right) The magnified image of the white-dotted square and layer by layer structure can be observed. (d) XRD results of the 40 nm thick pentacene film on BST.

of capacitance at low frequency can be attributed to the Maxwell–Wagner relaxations where the interface traps

linked to the oxygen vacancies in the film, and similar frequency dependence on capacitance have been reported in

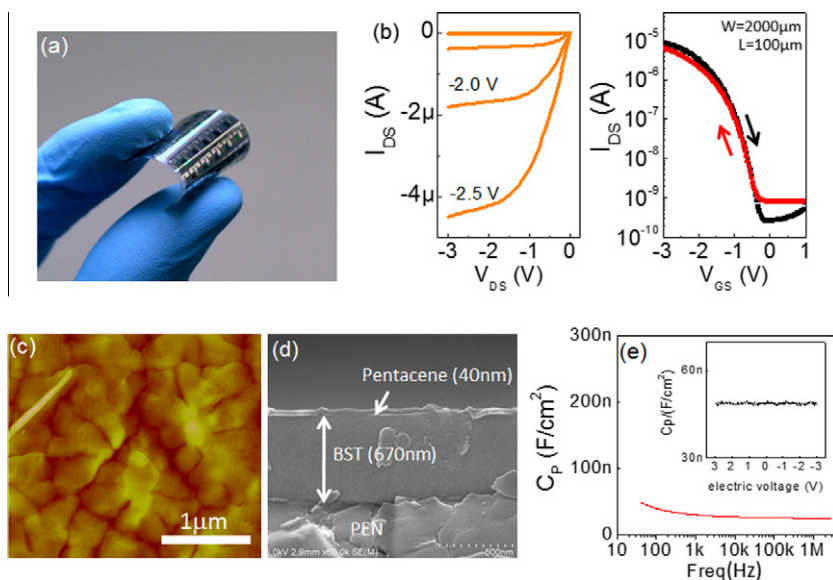
**Table 1**  
OTFT properties as a function of BST thickness on silicon substrate.

Thickness (nm)	Mobility ( $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ )	On/off	$V_{\text{th}}$ (V)	SS (mV/decade)
96	0.53	$4.88 \times 10^4$	-1.14	107
185	0.68	$8.13 \times 10^4$	-1.18	100
500	0.95	$7.45 \times 10^4$	-1.16	96.6
770	1.24	$1.30 \times 10^4$	-1.11	160

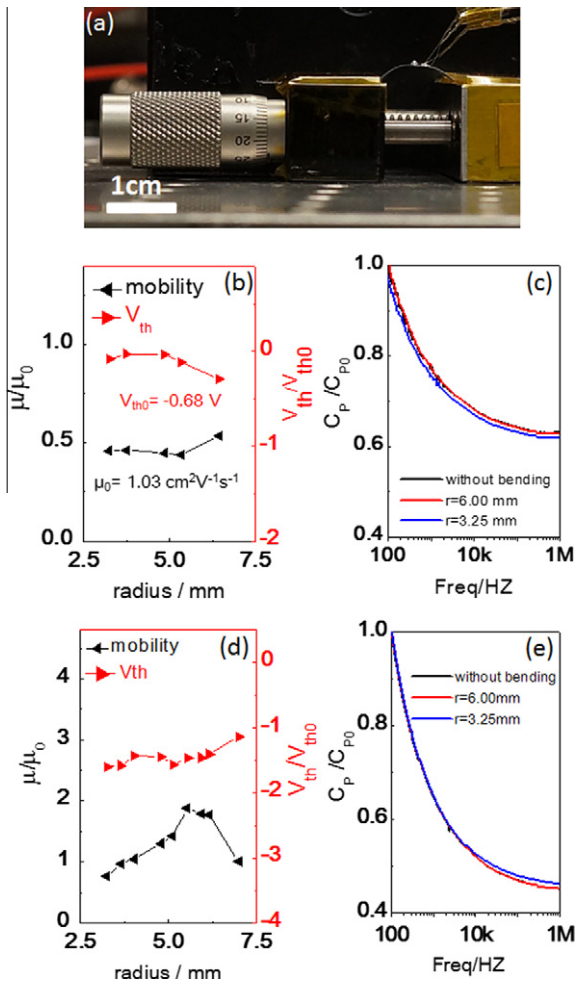
zirconia ( $\text{ZrO}_2$ ) film and titanium tantalum oxide (TiTaO) film by McIntyre and co-workers and Bertaud et al., respectively [22,23]. The thicker amorphous BST film also contributes more internal defects and oxygen deficiencies which would cause stronger space-charge polarization in the film and increase the capacitance at low frequency [24]. A detailed study of the relationship between the growth conditions such as pressure, temperature, laser power, morphology as well as film thicknesses to the capacitance of the BST thin films will be reported in the future work. The inset in Fig. 1(e) shows the  $C$ - $V$  measurement of the films at 40 Hz, the capacitance maintains a constant value over  $V = -3 \text{ V}$  to  $3 \text{ V}$  which suggests interface traps are not dominating in our samples.

The transfer and output characteristics curves of the OTFT with different BST thickness of 96 nm and 770 nm are shown in Fig. 2(a) and (b) respectively and the structure of the device is shown in the inset of Fig. 2(b). The characteristic curves show pinch off and current saturation in these OTFTs. In contrast to some of the solution processing which may generate unsaturated chemical bonds and causes trap states between the dielectric and semiconductor interface, we do not observe significant hysteresis effect in our devices due to the interface traps. By using the low frequency areal capacitances obtained from

extrapolation at low frequency in Fig. 1(e), the pentacene field effect mobilities ( $\mu_{\text{FE}}$ ) from the transfer curves in Fig. 2(b) are  $0.53 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  and  $1.24 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  respectively for the transistor based on 96 nm and 770 nm thick BST film. Different from multilayer silica dielectric where the mobility decreases significantly while the areal capacitance increases due to the broadening of the hole trap states under high polarizability [25], the mobilities of the current BST devices do not show a significant variation while the capacitance increases which suggests most of the extra charge traps are located inside the dielectric rather than the dielectric/semiconductor interface. Since the roughness of the BST films are almost the same, it suggests the mobility difference is not related to the dielectric surface roughness. A possible explanation for the mobility drop in the thinner BST film is the localization of the carriers due to the local dipole effect in the high- $k$  dielectric materials which hinders the mobility of the induced carriers [26]. The mobilities and other characteristic parameters including threshold voltage, subthreshold swing and on/off ratio of the pentacene OTFTs with different BST thicknesses on silicon substrate are listed in Table 1. These values are highly comparable with other high- $k$  metal oxides fabricated on silicon substrate by solution processing, atomic layer deposition or magnetron sputtering [8,9,16]. The high carrier mobility is attributed to the Stranski-Krastanov (S-K) growth mode of the pentacene where layer-plus-island structure can be observed in the AFM images shown in Fig. 2(c). The XRD spectrum of pentacene (Fig. 2(d)) confirms the highly crystallized pentacene islands in the thin film. It is also worth to mention that the low subthreshold swing (SS) in our devices suggests the trap state densities in between the pentacene and BST are low and it agrees with the fact that no hysteresis effect is observed.



**Fig. 3.** (a) The optical image of the OTFT on BST/PEN substrate. (b) The output and transfer characteristic curves of the device. (c) AFM image of the pentacene film on the BST/PEN. (d) Cross sectional SEM image of the BST thin film on the PEN substrate. (e)  $C$ - $f$  characteristic curve of the BST film on PEN. Inset:  $C$ - $V$  curve of the same film.



**Fig. 4.** (a) The picture of the upward bending setup for the flexible substrate. The variation of the mobility and threshold voltage of the flexible OTFT as a function of the (b) upward and (d) downward bending radius. The  $C$ - $f$  results of the BST thin film on PEN substrate under different (c) upward and (e) downward bending radii. The capacitances are normalized by the value at 100 Hz without bending.

In order to confirm the applications of low temperature PLD growth BST film on flexible substrate, we deposited the amorphous BST film on PEN substrate (125  $\mu\text{m}$ , Good Fellow, maximum operating temperature ca. 150  $^{\circ}\text{C}$ ) under the same conditions as the silicon based device (Fig. 3(a)) and a 100 nm thick of Ag is patterned as the bottom gate electrode. The output and transfer curves of the bottom gate flexible OTFT are shown in Fig. 3(b). Although the threshold voltage ( $-0.68$  V) and the on/off ratio ( $1.37 \times 10^4$ ) of the flexible device are comparable with the device on silicon, the subthreshold swing show degradation and the value is 260 mV/decade, while the field effect mobility is  $1.01 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . The mobility, threshold voltage and subthreshold swing of the current flexible devices are comparable with the previous reported result on flexible substrates [16,25,27,28], which shows the potential of using PLD for low temperature dielectric deposition. The relatively lower mobility in comparing with silicon substrate device could be attributed to the large surface

roughness of the PEN substrate (Fig. 3(d)) which hinders the interface contact between the bottom gate electrode and the BST film, and the pentacene layer. The AFM image of the pentacene on the BST/PEN also shows the dendritic structure is distorted (Fig. 3(c)) in comparing with the films grown on BST/silicon. Fig. 4(a) shows the picture of the experimental setup for the upward bending measurement on the BST/PEN OTFT. The variation of the normalized mobility and threshold voltage as a function of upward (convex) bending radius are shown in Fig. 4(b). The mobility of the device decreases with the bending radius and stabilized at around  $0.47 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  before a significant drop at below 3.25 mm. The mobility drop would possibly due to the increase of charge hopping distance in the pentacene layer under the tensile stress [29]. According to the equation for the strain ( $S$ )  $S = \frac{D}{2R}$  where  $D$  is the thickness of the film and  $R$  is the bending radius [30], the strain within the device is around 1.9% when the bending radius less is 3.25 mm. The strain is close to a value where buckling and delamination of electrodes may occur [31]. The normalized  $c$ - $f$  measurement results of a single BST dielectric thin film on PEN substrate under different bending radii are shown in Fig. 4(c). It can be noticed that the capacitance of the BST thin film is independent of the bending radius and thus the mobility drop in the device under bending is not due to the capacitance change of the dielectric layer. Furthermore, in the upward bending test, the threshold voltage is a little positively shifted and gets close to zero when the bending radius is getting smaller. It may be explained by the decrease of the trap states and contact resistance between pentacene/Ag electrodes due to tensile stress in metal electrodes. On the other hand, in the downward (concave) bending test results as shown in Fig. 4(d) and (e), the mobility of the device shows an increase with the bending radius up to 5.3 mm. The increase of the mobility is attributed to the reduction of the carrier hopping distance. The negatively shift of the threshold voltage is related to the increase of contact resistance when the electrodes under compressive stress. Fig. 4(e) shows that the capacitance of the dielectric is also independent of the bending radii under the downward bending test.

In conclusion, we demonstrated the feasibility of low temperature PLD growth BST thin film as the high- $k$  dielectric of the OTFT, we successfully fabricated pentacene based OTFT on silicon and PEN substrates with operating voltage less than 3 V. From the high resolution TEM and AFM image, we confirmed that the interface between silicon and BST is smooth and the pentacene layer shows excellent crystallization of islands with Stranski–Krastanov (S–K) growth mode. By transferring this dielectric growth method onto PEN flexible substrate, we demonstrated these OTFTs can operate with a voltage equals to 3 V with mobility  $1.01 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and subthreshold swing 260 mV/decade on flexible substrate. Also the bending test of the flexible device shows decent flexibility; the mobility can maintain at around  $0.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  or higher while the bending radius is around 3 mm for both upward and downward bending tests. These show the high application potentials of the low temperature PLD growth high- $k$  metal oxide for the flexible circuits and portable electronics.

## Acknowledgement

The work is supported by HKU (Code: 201109159013) and Poly (Code: J-BB9P).

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